

REMARKS

Claims 34-42 are in the application. Claims 1-33 have been cancelled.

By this amendment, applicants have amended claim 1. FIG. 4 supports that changes made to claim 1.

Response to 35 U.S.C. §112 Rejection

Claims 36 and 37 were rejected under 35 U.S.C. §112, first paragraph. Specifically, it was asserted that there is not support in applicants' specification that the upper surfaces of the pillar region are recessed below the major surface of the semiconductor substrate. This rejection is respectfully traversed in view of the remarks presented hereinafter.

Applicants respectfully submit that this element is described in their specification and drawing figures. Specifically, FIG. 2 shows dielectric material 60 deposited into recessed region 20 (see paragraph [0020]). Paragraph [0019] describes that dielectric material 60 is then subjected to a blanket and timed etch to remove a predetermined thickness, leaving dielectric material within recessed region to a level below dielectric layer 45. Paragraph [0019] further states that in one embodiment, the dielectric material etch back process is performed using reactive ion etching to a distance 48 below major surface 46 of semiconductor substrate 12.

As shown in FIGS. 3 and 4 and described in paragraph [0023], dielectric layer 60 subsequently becomes the array of pillars 65. And, as a natural consequence of dielectric

layer being below major surface 46, the dielectric pillars 65 will also be below the surface 46. This is clearly shown as well in FIG. 4 (note pillars 65 are shown in FIG. 4 with poly caps 75 overlying the upper surfaces thereof). Note that paragraphs [0009] and [0010] describe one embodiment of semiconductor substrate 12 to include both base layer 10 and epitaxial layer 30, and whether epitaxial layer 30 is there or not, element 46 is still the major surface of semiconductor substrate 12.

In view of the above highlighted support from applicants' specification and figures, applicants respectfully submit that claims 36 and 37 meet the requirements of §112, first paragraph.

#### Response to 35 U.S.C. §102 Rejections

Claims 34 and 38-41 were rejected under 35 U.S.C. §102(e) as being anticipated by Lur et al., USP 5,640,041. This rejection is traversed in view of the amendments made herein and the remarks presented hereinafter.

Claim 34 calls for, among other things, an intermediary of a semiconductor device including a pillar region comprising a dielectric material formed in the first recessed region and extending from the lower surface, wherein a void region is formed within the pillar region. Claim 34 also calls for a polysilicon cap layer formed overlying all upper-surfaces of the pillar region and aligned with the void region, wherein sidewall surfaces of the pillar region are devoid of the polysilicon cap layer, and wherein the pillar region, the polysilicon cap layer and the void region are configured to form an isolation region having reduced substrate capacitance.

Applicants first note that the Examiner points to Lur's FIG. 14 with reference to the gate layer 5. As is clearly set forth in Lur's specification at Col. 3, lines 58-60, FIG. 14 is "a completed integrated circuit". Thus, since claim 34 calls for an intermediary, FIG. 14 of Lur is not even relevant to the analysis.

Further, even if it was relevant, gate layer 5 is not configured to form an isolation region having reduced substrate capacitance. It merely sits on top of Lur's isolation region, but plays no part whatsoever in the formation of it. It is well accepted that functional language in claims must be given full weight and may not be disregarded in evaluating the patentability of the subject matter defined employing such functional language.

Hollister Inc. v E.R. Squibb & Sons, Inc., 902 F.2d 44, 14 U.S.P.Q.2d 2069, 2070 (Fed. Cir. 1990). The reliance on layer 5 in FIG. 14 disregards the functional language of claim 34, which is clearly inappropriate under current law.

Moreover, applicants have further amended claim 34 so that the polysilicon cap layer overlies all upper surfaces of the pillar region. As is clear in FIG. 14, gate layer 5 only overlies a portion of the finished isolation region. Additionally, in the claim 34 the polysilicon cap layer is aligned with the void region. Gate layer 5 in FIG. 14 is clearly not so oriented. Thus, for at least these reasons, applicants submit that Lur fails to anticipate claim 34.

Claims 38-41 depend from claim 34 and are believed allowable for at least the same reasons as claim 34.

Claims 35-37 and 42 were rejected under 35 U.S.C. §103(a) as being unpatentable over Lur. In view of the arguments presented above and the dependence of these claims on claim 34, applicants respectfully submit that claims 35-37 and 42 are allowable over Lur for at least the same reasons as claim 34.

In view of the above, it is believed that the claims are allowable, and the case is now in condition for allowance, which action is earnestly solicited.

Respectfully submitted,

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